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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/795,981	03/10/2004	Hisashi Nagata	1035-499	2189
23117	7590	11/15/2005	EXAMINER DUONG, THOI V	
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			ART UNIT 2871	PAPER NUMBER

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

1. This office action is in response to the Amendment filed August 30, 2005.

Accordingly, claims 12 and 35 were amended, and claims 1-8, 16-27, 29-34 and 38-41 were cancelled. Currently, claims 9-15, 28, 35-37 and 42 are pending in this application.

Claim Objections

2. Claim 12 is objected to because of the following informalities: claim 12 should be labeled as "Amended" instead of "Previously presented". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

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4. Claims 9-13 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Jung Mok et al. (Jung Mok, USPN 5,923,390).

Re claim 9, as shown in Figs. 4-6, Jung Mok discloses an active matrix substrate, comprising:

- a pixel electrode 87(93) provided in a pixel area;

- a scanning line 60 and a signal line 70;

- a switching element electrically connected to the scanning line 60, the signal line 70, and the pixel electrode 87(93),

- a storage capacitor electrode 81b for a storage capacitor; and

- a storage capacitor common wire 91 disposed parallel to the signal line so as to be electrically connected to the storage capacitor electrode 81b, wherein

- storage capacitance is provided between the pixel electrode 87 and the storage capacitor electrode 81b,

- the scanning line 60(81a) and the storage capacitor electrode 81b are fabricated from a same material in a single patterning (col. 6, lines 1-6); and

- wherein the storage capacitor electrode 81b and the storage capacitor common wire 91 are patterned in different steps so as to have an insulating film 82 provided partially therebetween (col. 8, lines 18-23).

Re claims 10, 12 and 42, the signal line 70 and the pixel electrode 87 and the storage capacitor common wire 91 are fabricated from a single conductive layer through patterning thereof (col. 6, lines 23-30).

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Re claim 11, the active matrix substrate of Jung Mok further comprises an interlayer insulation film 92 on which the pixel electrode 93 is provided.

Re claim 13, the active matrix substrate of Jung Mok further comprises a gate insulating film 82 for covering a gate electrode 81a of the switching element TFT, wherein the pixel electrode 87 is disposed opposing the storage capacitor electrode across the gate insulation film 82.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 14, 15 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung Mok et al. (Jung Mok, USPN 5,923,390) in view of Oh et al. (Oh, USPN 6,211,928 B1).

Re claim 14, as shown in Figs. 4-6, Jung Mok discloses an active matrix substrate, comprising:

a pixel electrode 87(93) provided in a pixel area;

a scanning line 60 and a signal line 70;

a switching element electrically connected to the scanning line 60, the signal line 70, and the pixel electrode 87(93),

a storage capacitor electrode 81b for a storage capacitor; and

a storage capacitor common wire 91 disposed parallel to the signal line so as to be electrically connected to the storage capacitor electrode 81b, wherein

storage capacitance is provided between the pixel electrode 87 and the storage capacitor electrode 81b,

the scanning line 60(81a) and the storage capacitor electrode 81b are fabricated from a same material in a single patterning (col. 6, lines 1-6); and

a protection film 92 for covering the switching element.

Jung Mok discloses an active matrix substrate that is basically the same as that recited in claim 14 except for an interlayer insulation film interposed between the pixel electrode and the protection film.

As shown in Fig. 8J, Oh discloses an active matrix substrate comprising a protection film 126 (passivation film), a pixel electrode 104, and an insulation film 156 (planarization film) interposed between the pixel electrode 104 and the protection film 126.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the active matrix substrate of Bae with the teaching of Oh by forming an interlayer insulating film interposed between the pixel electrode and the protection film to obtain a smooth surface profile and improve aperture ratio (col. 6, lines 53-59).

Re claim 15, as shown in Fig. 8J, a contact hole is formed through the interlayer insulation film 156 and the protection film 126 so as to electrically connecting the pixel electrode 104 to the switching element.

Re claim 28, as shown in Fig. 8J, Oh discloses that the scanning line 117a is anodized to form an anodized film 135 to prevent hillocks and improve electrical insulation (col. 5, lines 9-12).

7. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung Mok et al. (Jung Mok, USPN 5,923,390) in view of Jeromin et al. (8.4: Application of a-Si Active-Matrix Technology in a X-Ray Detector Panel).

Re claim 35, as shown in Figs. 4-6, Jung Mok discloses an active matrix substrate, comprising:

- a pixel electrode 87(93) provided in a pixel area;
 - a scanning line 60 and a signal line 70;
 - a switching element electrically connected to the scanning line 60, the signal line 70, and the pixel electrode 87(93),
 - a storage capacitor electrode 81b for a storage capacitor; and
 - a storage capacitor common wire 91 disposed at least partially parallel to the signal line so as to be electrically connected to the storage capacitor electrode 81b,
- wherein
- the scanning line 60(81a) and the storage capacitor electrode 81b are fabricated from a same material in a single patterning (col. 6, lines 1-6); and
 - wherein the storage capacitor electrode 81b and the storage capacitor common wire 91 are patterned in different steps so as to have an insulating film 82 provided partially therebetween (col. 8, lines 18-23).

Re claim 36, Jung Mok further discloses a gate insulation film 82 for covering a gate electrode 81a of the switching element; and a conductive body layer 87 deposited on the gate insulation film 82 so as to be connected to the switching element, wherein the storage capacitor electrode 81b and the conductive body layer 87 constitute the storage capacitor across the gate insulation film.

Jung Mok discloses an active matrix substrate that is basically the same as that recited in claim 34 except for an image sensor comprising a conversion section for converting incident magnetoelectric radiation to electric charges and bias voltage application means for causing a storage capacitor to store the electric charges.

In "Application of a-Si Active-Matrix Technology in a X-Ray Detector Panel" cited by Applicant, Jeromin discloses an active matrix substrate used in X-ray detector panel comprising amorphous selenium which converts x-ray photons into charge carrier pairs. Jeromin also discloses that the positive charges are collected in the storage capacitors of the pixels and are then read out charge amplifiers connected to the source lines (see Abstract). Accordingly, a conversion section for converting incident magnetoelectric radiation to electric charges and bias voltage application means for causing a storage capacitor to store the electric charges are to be employed in the X-Ray detector panel.

Since the active matrix substrate of Jung Mok provides high aperture ratio without decrease in storage capacitance (Jung Mok, col. 2, lines 32-34), as intended purpose, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the active matrix substrate of Jung Mok in the image sensor of Jeromin comprising a conversion section for converting incident

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magnetoelectric radiation to electric charges and bias voltage application means for causing a storage capacitor to store the electric charges for obtaining the actual x-ray image (page 93, col. 2).

8. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jung Mok et al. (Jung Mok, USPN 5,923,390) in view of Jeromin et al. (8.4: Application of a-Si Active-Matrix Technology in a X-Ray Detector Panel) as applied to claims 35-37 above and further in view of Oh et al. (Oh, USPN 6,211,928 B1).

Jung Mok as modified in view of Jeromin above includes all that is recited in claim 38 except for the scanning line being anodized.

As shown in Fig. 8J, Oh discloses that the scanning line 117a is anodized to form an anodized film 135 to prevent hillocks and improve electrical insulation (col. 5, lines 9-12).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the active matrix substrate of Jung Mok with the teaching of Oh by anodizing the scanning line to prevent hillocks and improve electrical insulation (col. 5, lines 9-12).

Response to Arguments

9. Applicant's arguments filed August 30, 2005 have been fully considered but they are not persuasive.

Applicant argued that Jung Mok fails to disclose or suggest "the storage capacitor common wire disposed at least partially parallel to the signal line" as recited in claims 9, 12, 14, 35 and 42. The Examiner disagrees since Fig. 4 of Jung Mok clearly

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shows that the storage capacitor common wire 91 (not 81b) is disposed at least partially parallel to the signal line 70 since the storage capacitor common wire 91 is elongated along the signal line 70.

Applicant also argued that one of ordinary skill in the art would readily recognize that transparent pixel electrode 91 cannot be considered a "storage capacitor common wire" and 91 cannot be considered "parallel" to the signal line. The Examiner disagrees with Applicant's remarks. Although Jung Mok names 91 is a first transparent pixel electrode, it functions as a pixel capacitor wire which forms a first storage capacitance SC1 with a second transparent pixel electrode 93, wherein the second transparent pixel electrode 93 contacts the drain electrode 85 of the thin film transistor 80 as shown in Figs. 5 and 6. Thus, 91 can be considered as a "storage capacitor common wire". Moreover, since the storage capacitor common wire 91 is spaced apart by a selected distance from the signal line 70 (col. 4, lines 37-42) and elongated along the signal line 70 as shown in Fig. 4, the storage capacitor common wire 91 is considered "parallel" to the signal line 70.

Further, Applicant argued that Jung Mok fails to disclose or suggest "the storage capacitor electrode and the storage capacitor common wire being patterned in different steps so as to have an insulation film provided partially therebetween". The Examiner disagrees since Fig. 5 of Jung Mok clearly shows a storage capacitor electrode 81b formed on the substrate 200, an insulating layer 82 formed on the storage capacitor electrode 81b and a storage capacitor common wire 91 formed on the insulating layer 82 (col. 4, line 65 through col. 5, line 9). In addition, as to the product-by-process

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limitation "the storage capacitor electrode and the storage capacitor common wire being patterned in different steps", it has been recognized that "Even through product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art product was made by a different process". *In re Thorpe*, 227 USPQ 964,966 (Fed. Cir. 1985). See also MPEP 2113.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-

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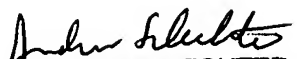
2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong



11/12/2005


ANDREW SCHECHTER
PRIMARY EXAMINER